

NCR65C02

■ AC CHARACTERISTICS $V_{DD} = 5.0V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$, Load = 1 TTL + 130 pF

Parameter	Symbol	1MHz		2MHz		3MHz		Unit
		Min	Max	Min	Max	Min	Max	
Delay Time, θ_0 (IN) to θ_2 (OUT)	t_{DLY}	—	60	—	60	20	60	nS
Delay Time, θ_1 (OUT) to θ_2 (OUT)	t_{DLY1}	-20	20	-20	20	-20	20	nS
Cycle Time	t_{CYC}	1.0	5000*	0.50	5000*	0.33	5000*	μS
Clock Pulse Width Low	t_{PL}	460	—	220	—	160	—	nS
Clock Pulse Width High	t_{PH}	460	—	220	—	160	—	nS
Fall Time, Rise Time	t_F, t_R	—	25	—	25	—	25	nS
Address Hold Time	t_{AH}	20	—	20	—	0	—	nS
Address Setup Time	t_{ADS}	—	225	—	140	—	110	nS
Access Time	t_{ACC}	650	—	310	—	170	—	nS
Read Data Hold Time	t_{DHR}	10	—	10	—	10	—	nS
Read Data Setup Time	t_{DSU}	100	—	60	—	60	—	nS
Write Data Delay Time	t_{MDS}	—	30	—	30	—	30	nS
Write Data Hold Time	t_{DHW}	20	—	20	—	15	—	nS
\overline{SO} Setup Time	t_{SO}	100	—	100	—	100	—	nS
Processor Control Setup Time**	t_{PCS}	200	—	150	—	150	—	nS
SYNC Setup Time	t_{SYNC}	—	225	—	140	—	100	nS
ML Setup Time	t_{ML}	—	225	—	140	—	100	nS
Input Clock Rise/Fall Time	t_{F0}, t_{R0}	—	25	—	25	—	25	nS

*NCR65C02 can be held static with θ_2 high.

**This parameter must only be met to guarantee that the signal will be recognized at the current clock cycle.

■ MICROPROCESSOR OPERATIONAL ENHANCEMENTS

Function	NMOS 6502 Microprocessor	NCR65C02 Microprocessor																					
Indexed addressing across page boundary.	Extra read of invalid address.	Extra read of last instruction byte.																					
Execution of invalid op codes.	Some terminate only by reset. Results are undefined.	All are NOPs (reserved for future use). <table> <tr> <th>Op Code</th><th>Bytes</th><th>Cycles</th></tr> <tr> <td>X2</td><td>2</td><td>2</td></tr> <tr> <td>X3, X7, XB, XF</td><td>1</td><td>1</td></tr> <tr> <td>44</td><td>2</td><td>3</td></tr> <tr> <td>54, D4, F4</td><td>2</td><td>4</td></tr> <tr> <td>5C</td><td>3</td><td>8</td></tr> <tr> <td>DC, FC</td><td>3</td><td>4</td></tr> </table>	Op Code	Bytes	Cycles	X2	2	2	X3, X7, XB, XF	1	1	44	2	3	54, D4, F4	2	4	5C	3	8	DC, FC	3	4
Op Code	Bytes	Cycles																					
X2	2	2																					
X3, X7, XB, XF	1	1																					
44	2	3																					
54, D4, F4	2	4																					
5C	3	8																					
DC, FC	3	4																					
Jump indirect, operand = XXFF.	Page address does not increment.	Page address increments and adds one additional cycle.																					
Read/modify/write instructions at effective address.	One read and two write cycles.	Two read and one write cycle.																					
Decimal flag.	Indeterminate after reset.	Initialized to binary mode (D=0) after reset and interrupts.																					
Flags after decimal operation.	Invalid N, V and Z flags.	Valid flag adds one additional cycle.																					
Interrupt after fetch of BRK instruction.	Interrupt vector is loaded, BRK vector is ignored.	BRK is executed, then interrupt is executed.																					

■ MICROPROCESSOR HARDWARE ENHANCEMENTS

Function	NMOS 6502	NCR65C02
Assertion of Ready RDY during write operations.	Ignored.	Stops processor during θ_2 .
Unused input-only pins (\overline{IRO} , \overline{NMI} , \overline{RDY} , \overline{RES} , \overline{SO}).	Must be connected to low impedance signal to avoid noise problems.	Connected internally by a high-resistance to V_{DD} (approximately 250 K ohm.)